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# BIOSTAR GROUP


## N68SC-M3S

VER:6.1

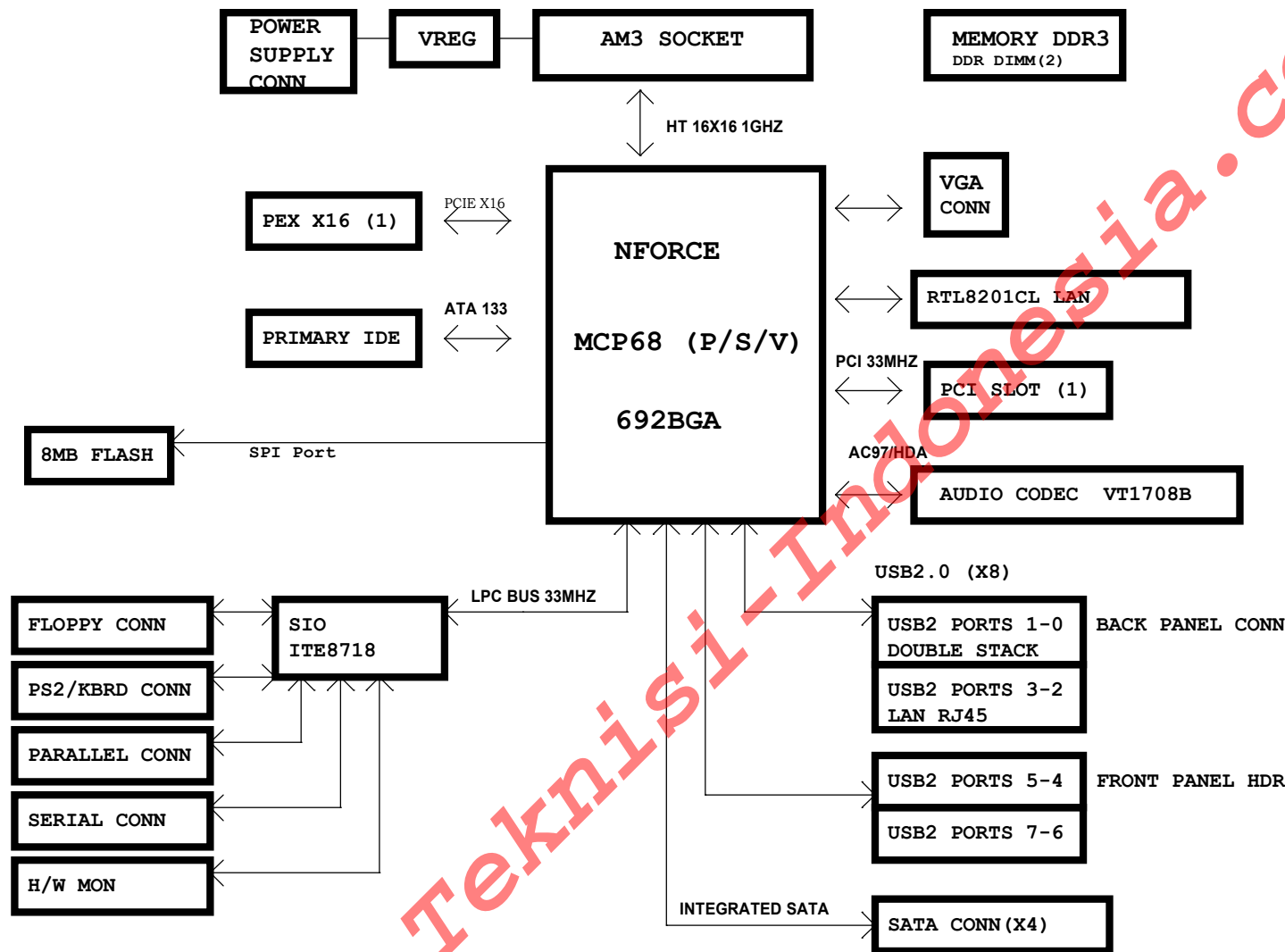
## AM3 & MCP68S


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Title COVER SHEET		
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# N68SC-M3S Block Diagram



 <b>映泰股份有限公司</b> <b>BIOSTAR GROUP</b>		
Title <b>SYSTEM BLOCK</b>		
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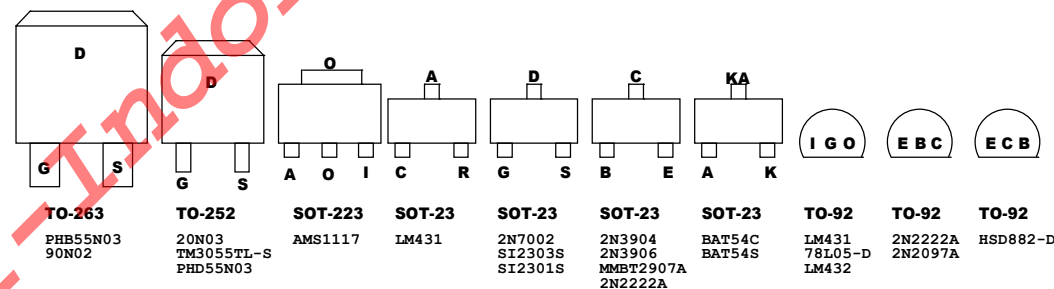
CPU VID TABLE			
VID [4..0]	VDD	VID [4..0]	VDD
0X00000	1.550V	0X10000	1.150V
0X00001	1.525V	0X10001	1.125V
0X00010	1.500V	0X10010	1.100V
0X00011	1.475V	0X10011	1.075V
0X00100	1.450V	0X10100	1.050V
0X00101	1.425V	0X10101	1.025V
0X00110	1.400V	0X10110	1.000V
0X00111	1.375V	0X10111	0.975V
0X01000	1.350V	0X11000	0.950V
0X01001	1.325V	0X11001	0.925V
0X01010	1.300V	0X11010	0.900V
0X01011	1.275V	0X11011	0.875V
0X01100	1.250V	0X11100	0.850V
0X01101	1.225V	0X11101	0.825V
0X01110	1.200V	0X11110	0.800V
0X01111	1.175V	0X11111	OFF

SMBUS ADDRESS MAP		
DEVICE	SMBUS #	ADDRESS
SLOT		
DIMM 0	0	1010 000 = 0X50
DIMM 1	0	1010 001 = 0X51
DIMM 2	0	1010 010 = 0X52
DIMM 3	0	1010 011 = 0X53
SIO	1	0101 101 = 0X2D
PCI SLOT 1	1	ARP
PCI SLOT 2	1	ARP
PCI SLOT 3	1	ARP
PCI SLOT 4	1	ARP
DDC BUS	A	?
DDC BUS	B	?

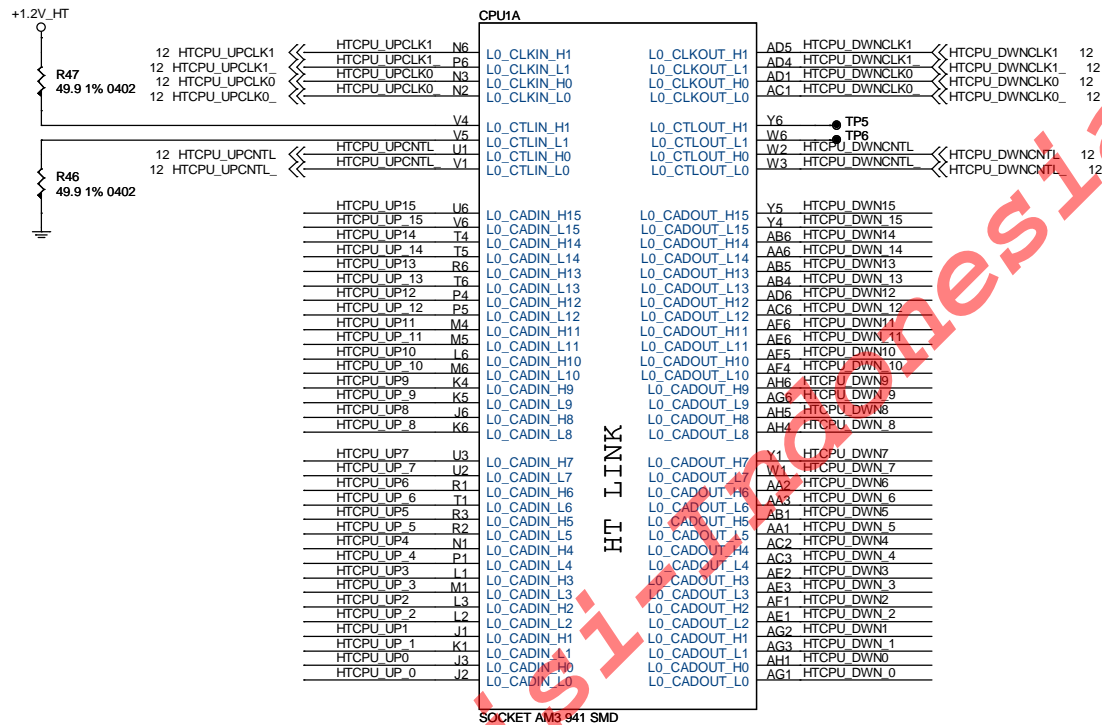
22U/25DE	5"7 mm
100U/16DE	6.3"11 mm
220U/10DE	6.3"11 mm
470U/16DE	8"11 mm
1000U/10DE	8"14 mm
1500U/16DE	10"25 mm
3300U/25DE	10"25 mm

PCI INTERRUPT/IDSEL MAP								
BACK PANEL SLOT	PCI BUS#	DEVICE#	IDSEL PIN	PCI SLOT INTA*	PCI SLOT INTB*	PCI SLOT INTC*	PCI SLOT INTD*	REQ/GNT
1	01	0X05	22	P INTY*	P INTZ*	P INTW*	P INTX*	1/1
2	01	0X06	24	P INTW*	P INTX*	P INTY*	P INTZ*	2/2
3	01	0X07						
4	01	0X08						
5	01	0X09						
6	01	0X0A						

PCI DEVICE MAP				
DEVICE	PCI BUS#	FUNCTION	IDSEL PIN	DEVICE ID
MCP61P	MCP61 LOGICAL PCI BUS 0	0X01-0X0F	--	--
MAC /MAC	0	XA	0	0X56/57
PCI-PCI BRIDGE	0	X9	0	0X005C
SATA1	0	X8	0	0X0055
SATA0	0	X8	0	0X0054
IDE	0	X6	0	0X0053
MODEM CODEC	0	X4	1	0X0058
AUDIO CODEC	0	X4	0	0X0059
USB 2.0	0	X2	1	0X005B
USB 1.1	0	X2	0	0X005A
SHAPE TRIM	0	X1	2	0X005F
LDT	0	X0	0	0X005E
SMBUS2	0	X1	1	0X0052
LEGACY SLAVE	0	?	?	0X00D3
LPC	0	X1	0	0X0050/51
LOGICAL PCI BUS	1	?	?	?
PCI SLOT 1				
PCI SLOT 2				
PCI SLOT 3				
PCI SLOT 4				
PCI SLOT 5				

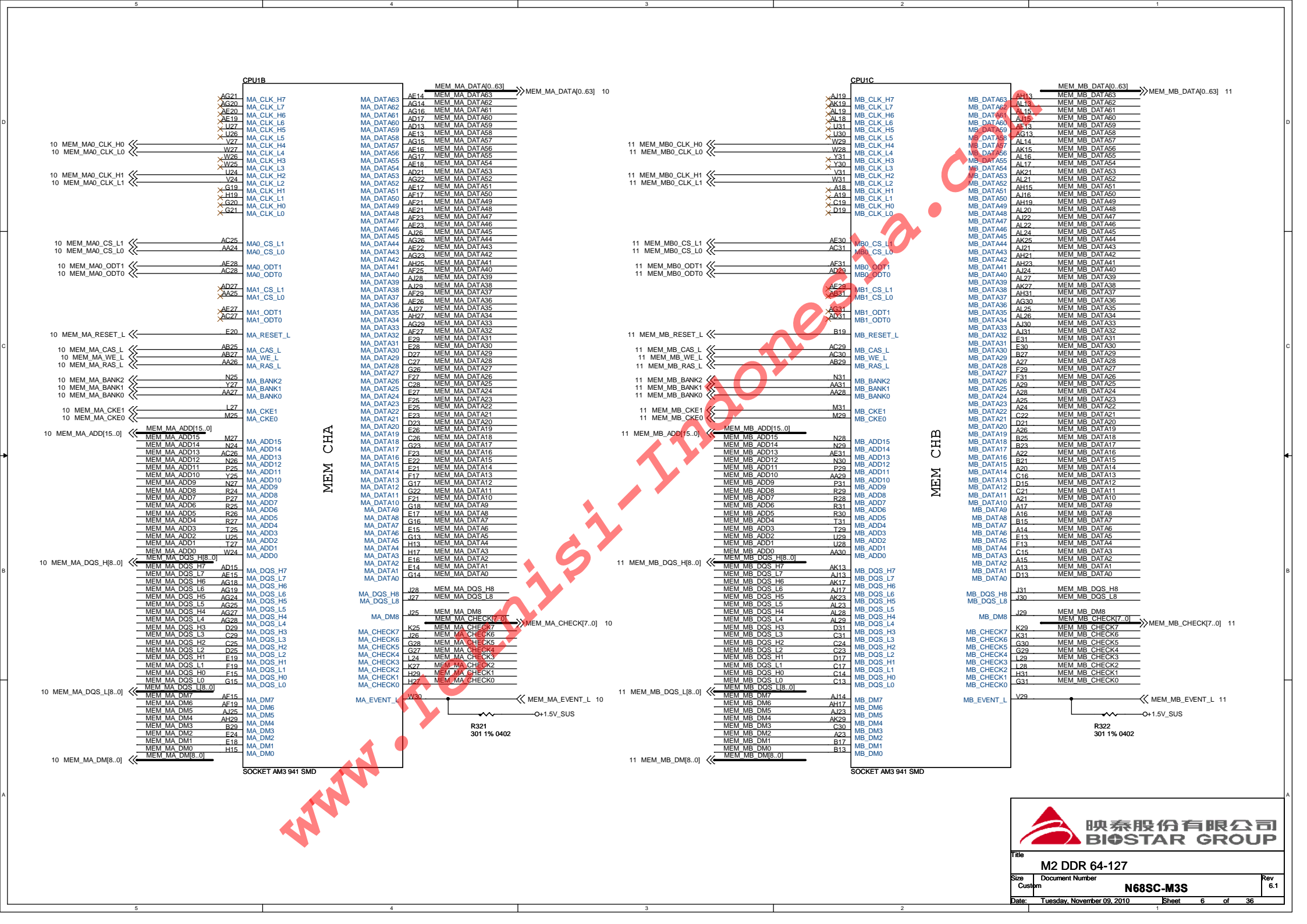


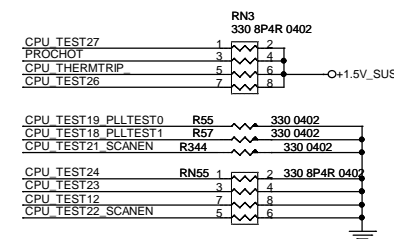
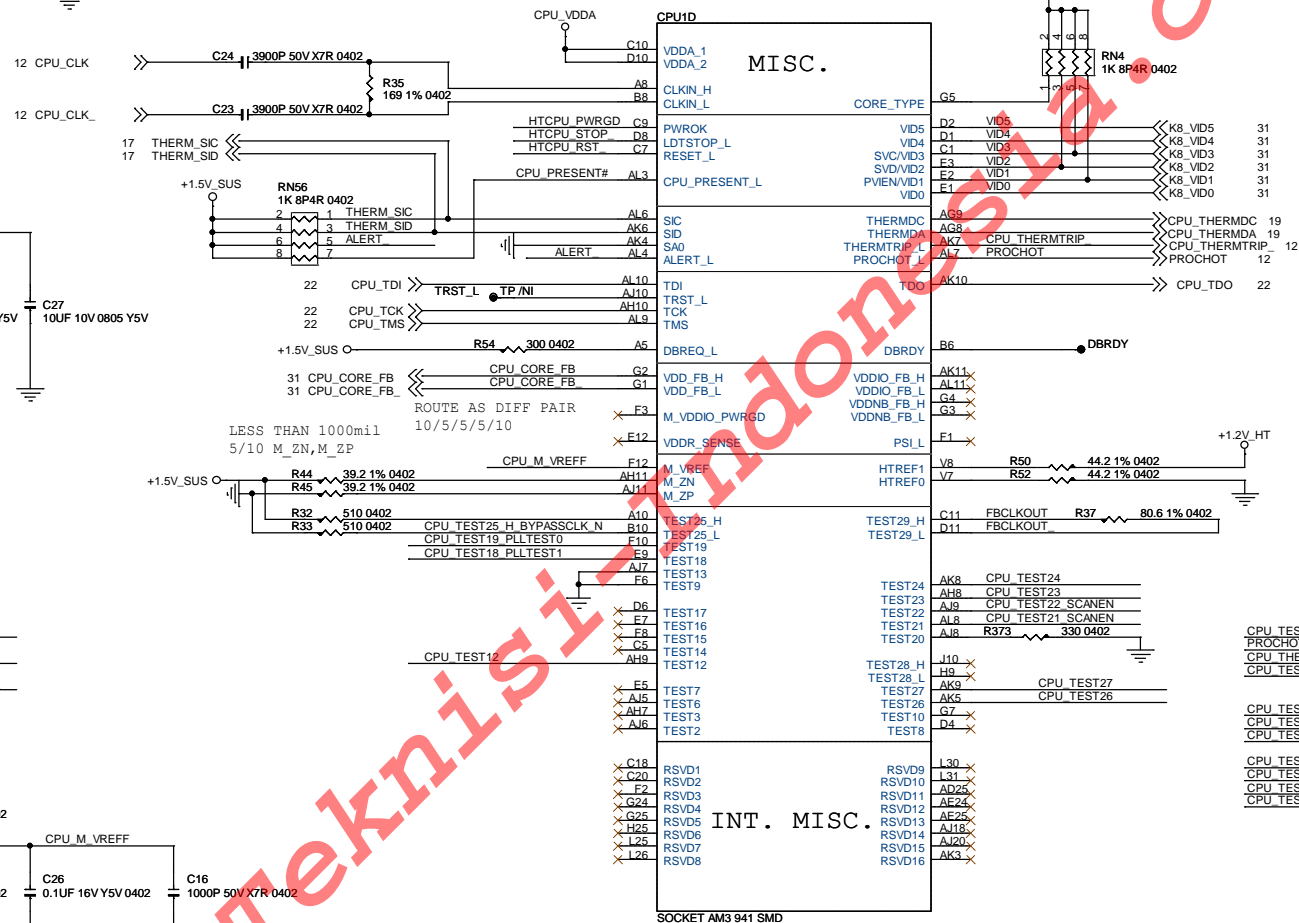
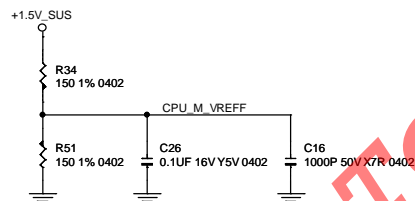
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		SPEC&CHANGE LIST	
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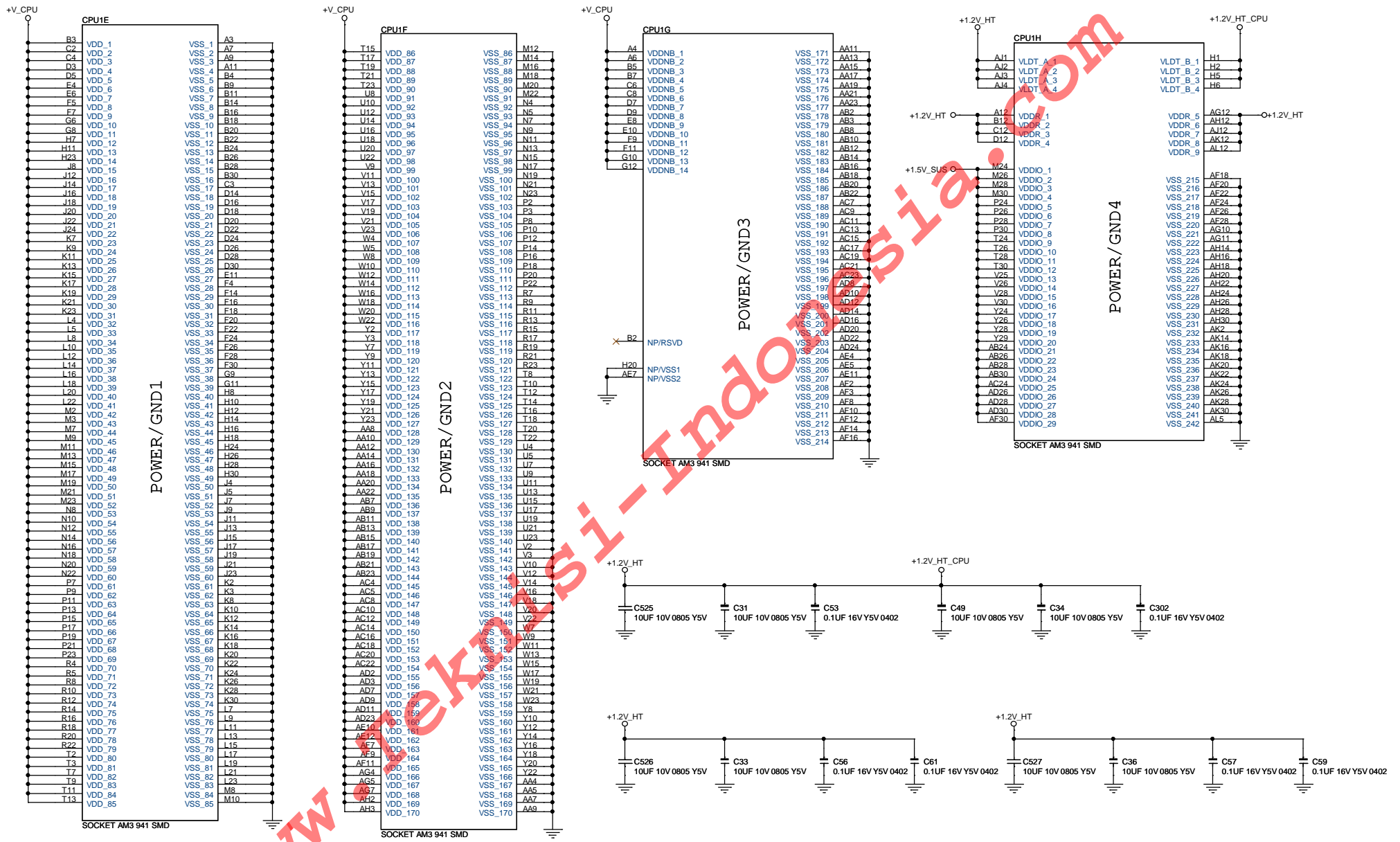


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 12 HTCPU\_UP\_15..0 << HTCPU\_UP\_15..0

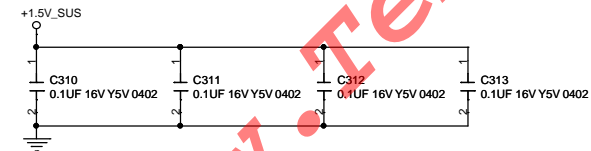
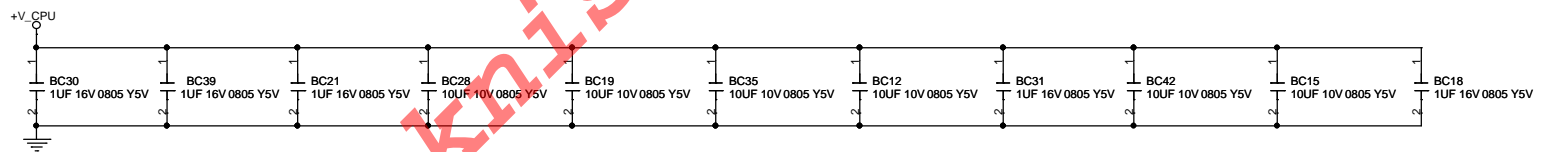
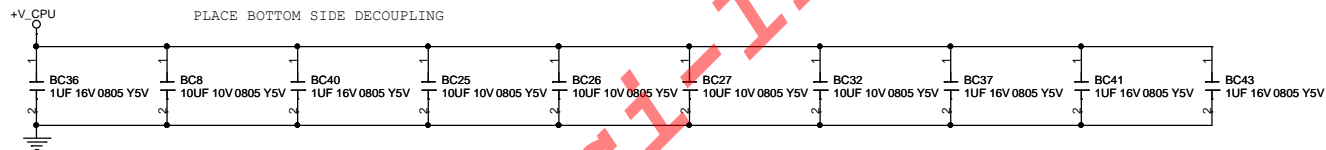
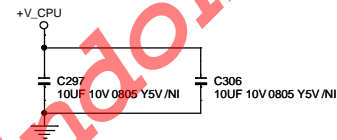
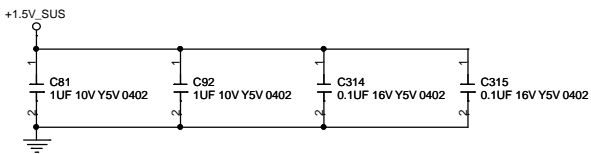
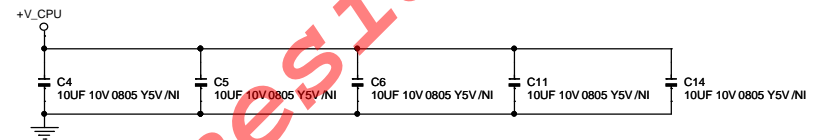
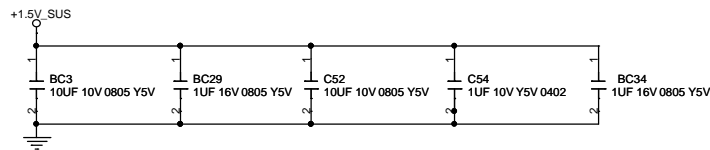
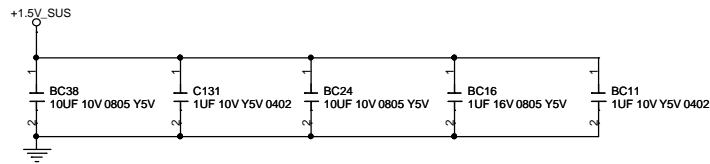
HTCPU\_DWN[15..0] << HTCPU\_DWN[15..0] 12  
 HTCPU\_DWN\_15..0 << HTCPU\_DWN\_15..0 12



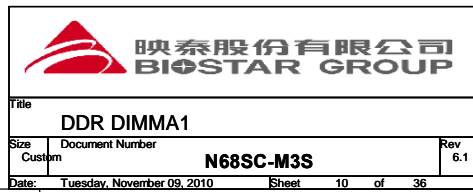




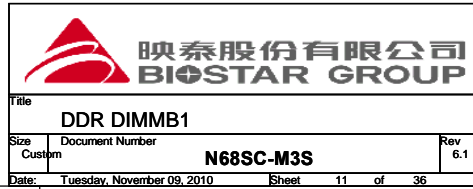




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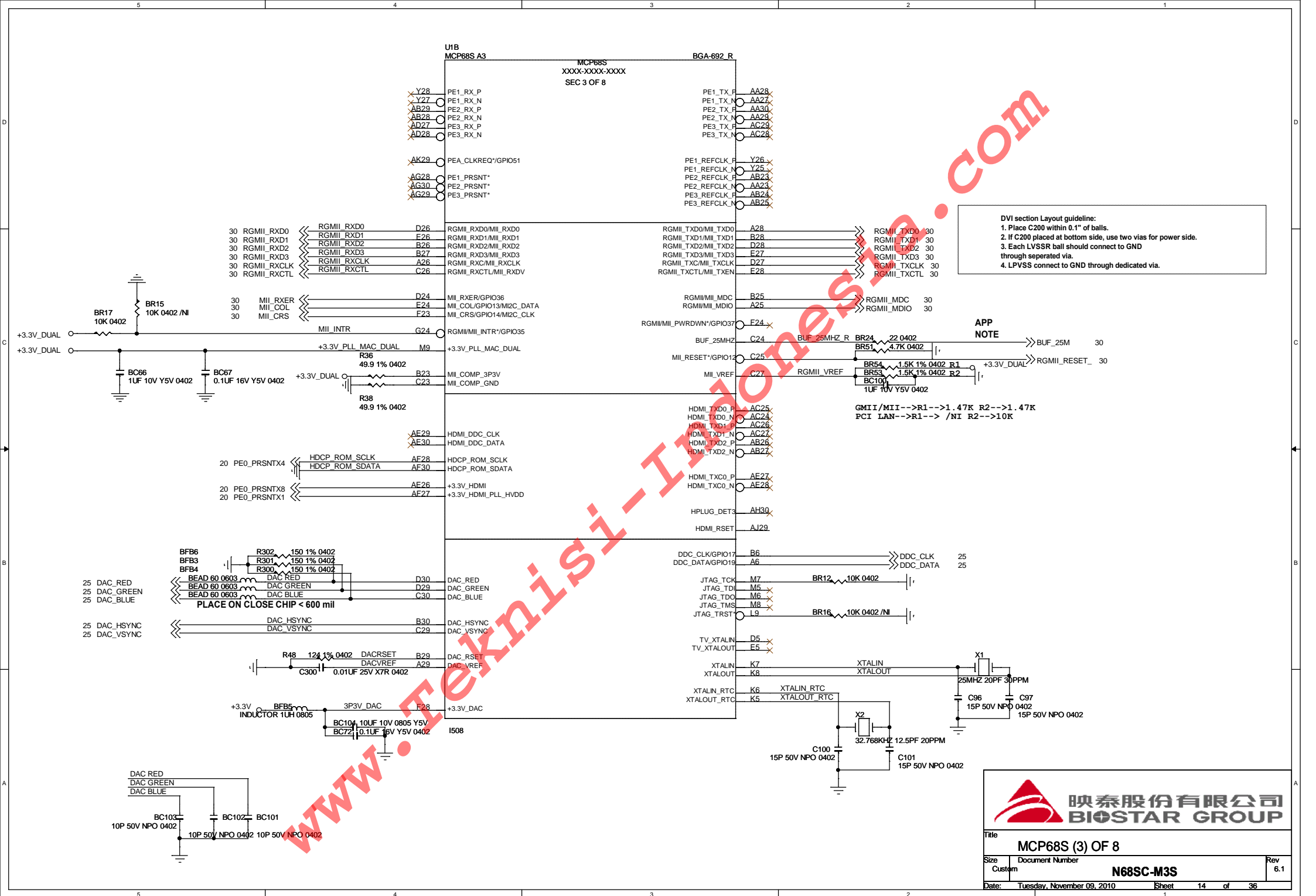


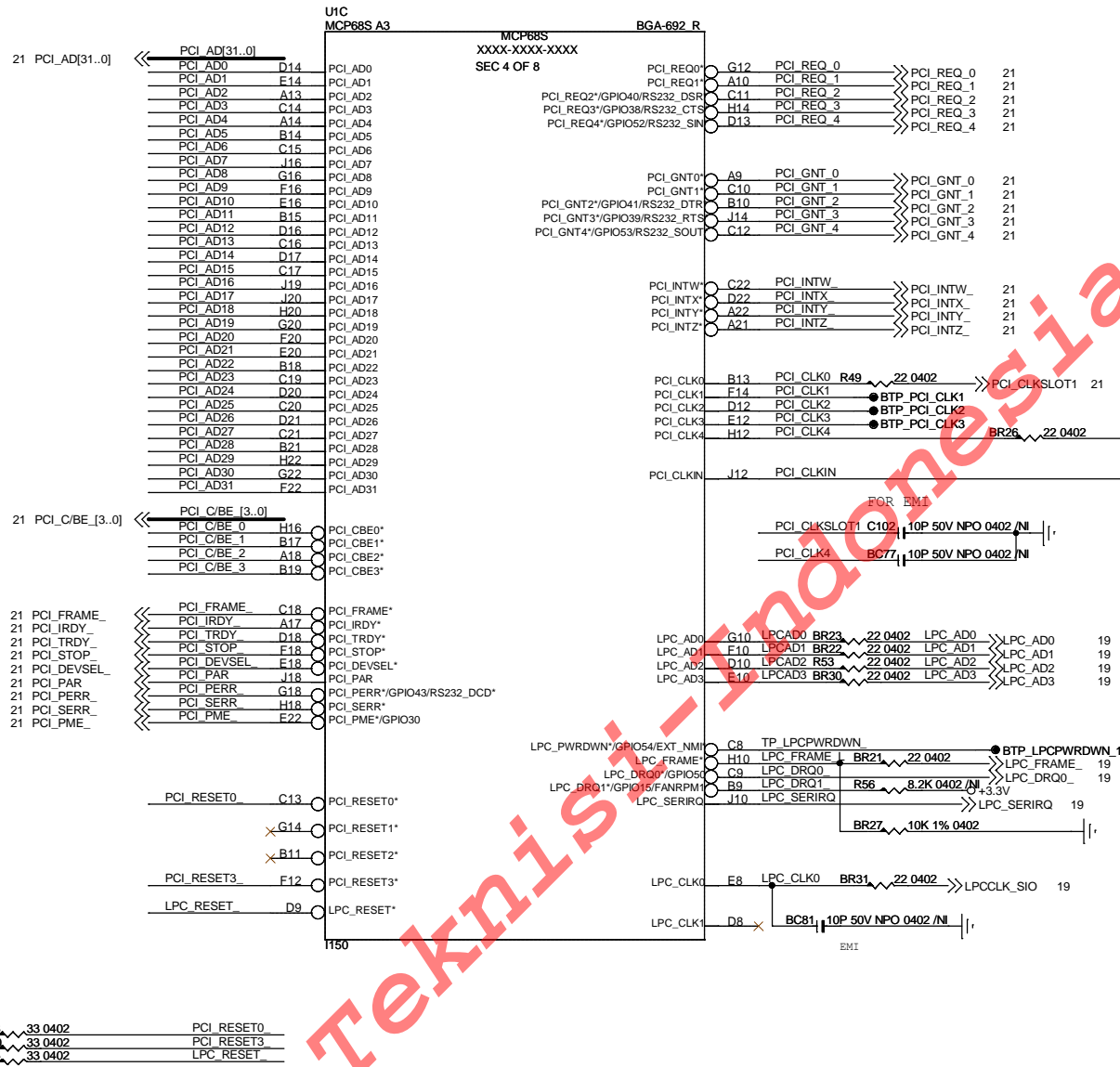
**A9** **BLACK**












HDA\_SDOU18  
LPC\_FRAME

0 0 = LPC BIOS 1-2 DEFAULT  
0 1 = PCI BIOS 2-3  
1 0 = SPI BIOS 1-2  
1 1 = RESERVED

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Title  
MCP68S (4) OF 8

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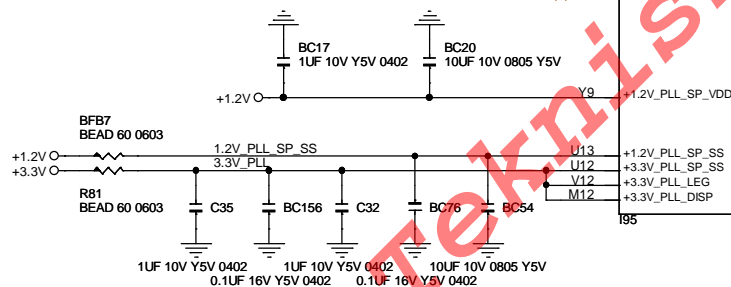
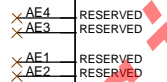
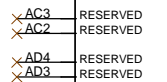
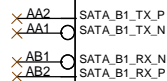
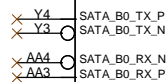
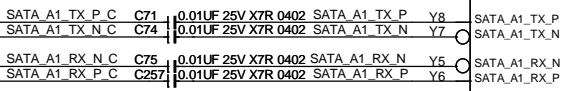
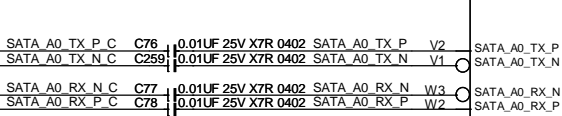
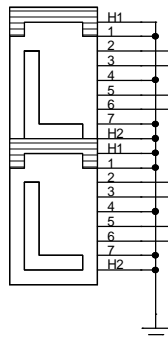
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SATA1  
SATA CONNECTOR-R

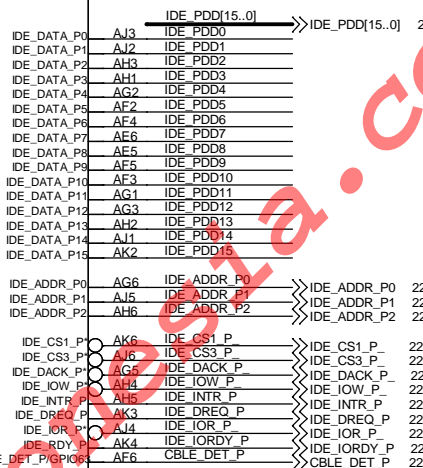
SATA2  
SATA CONNECTOR-R




U1D  
MCP68S A3

MCP68S  
XXXX-XXXX-XXXX  
SEC 5 OF 8

BGA-692 R



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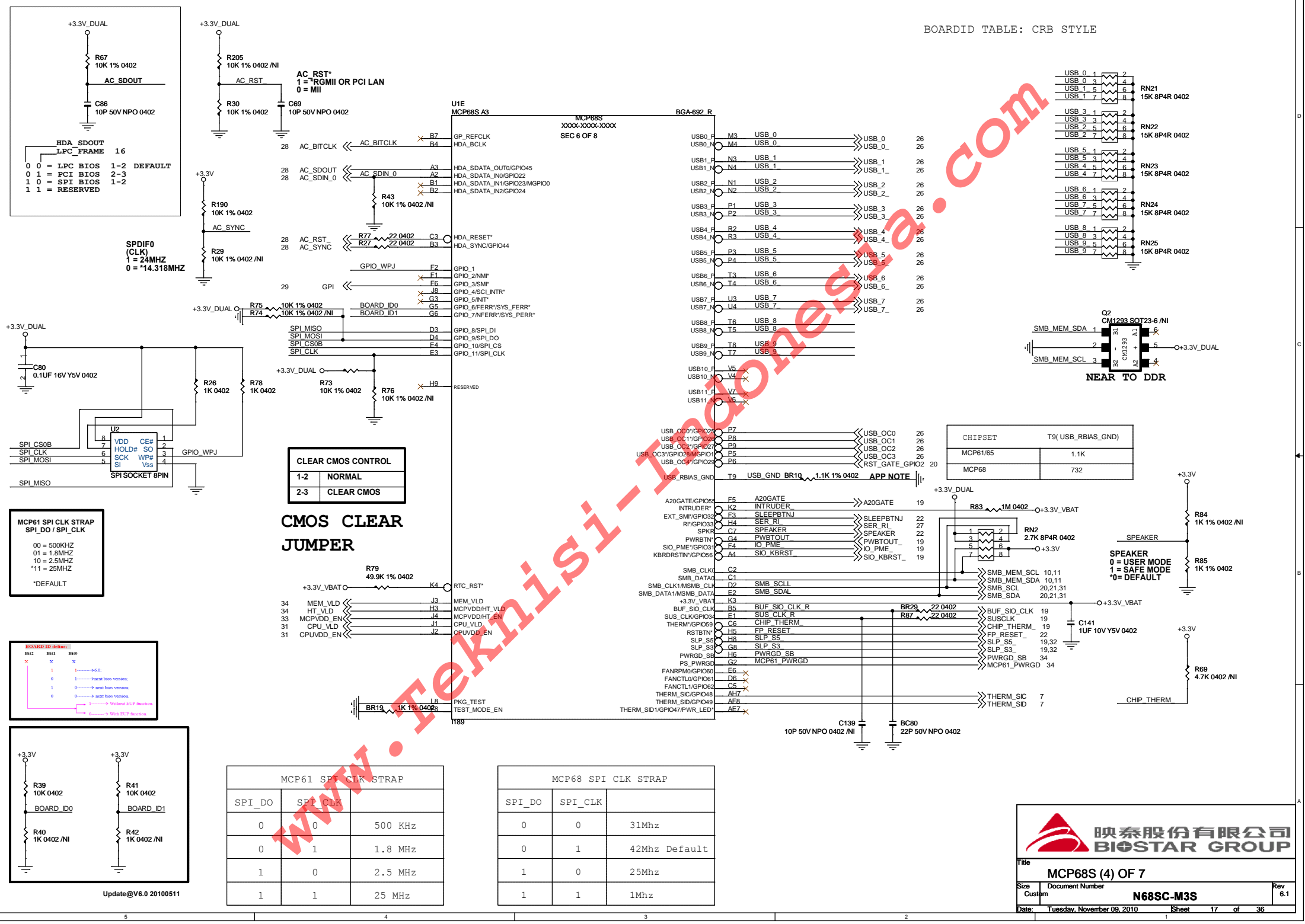
Title  
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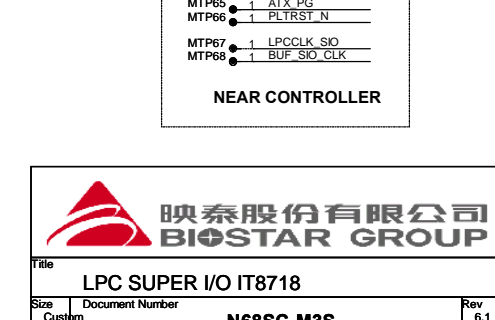
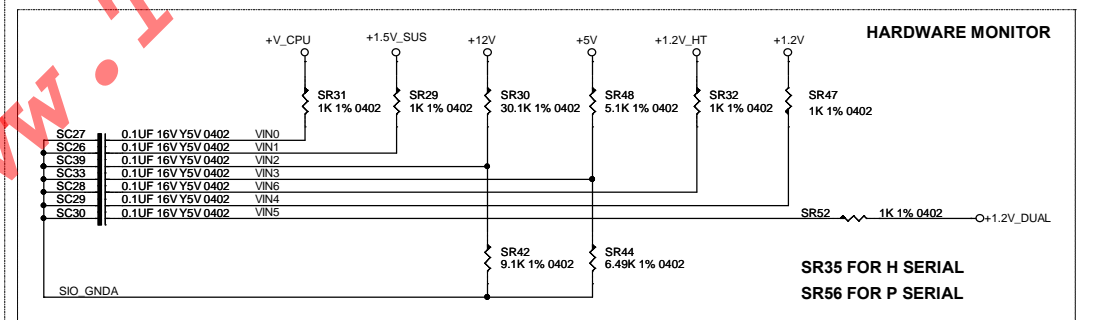
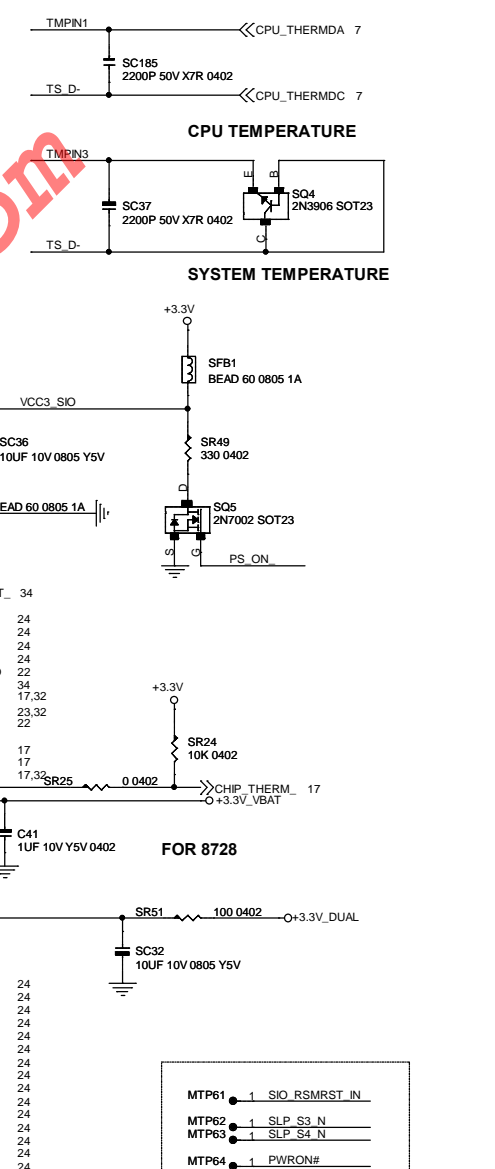
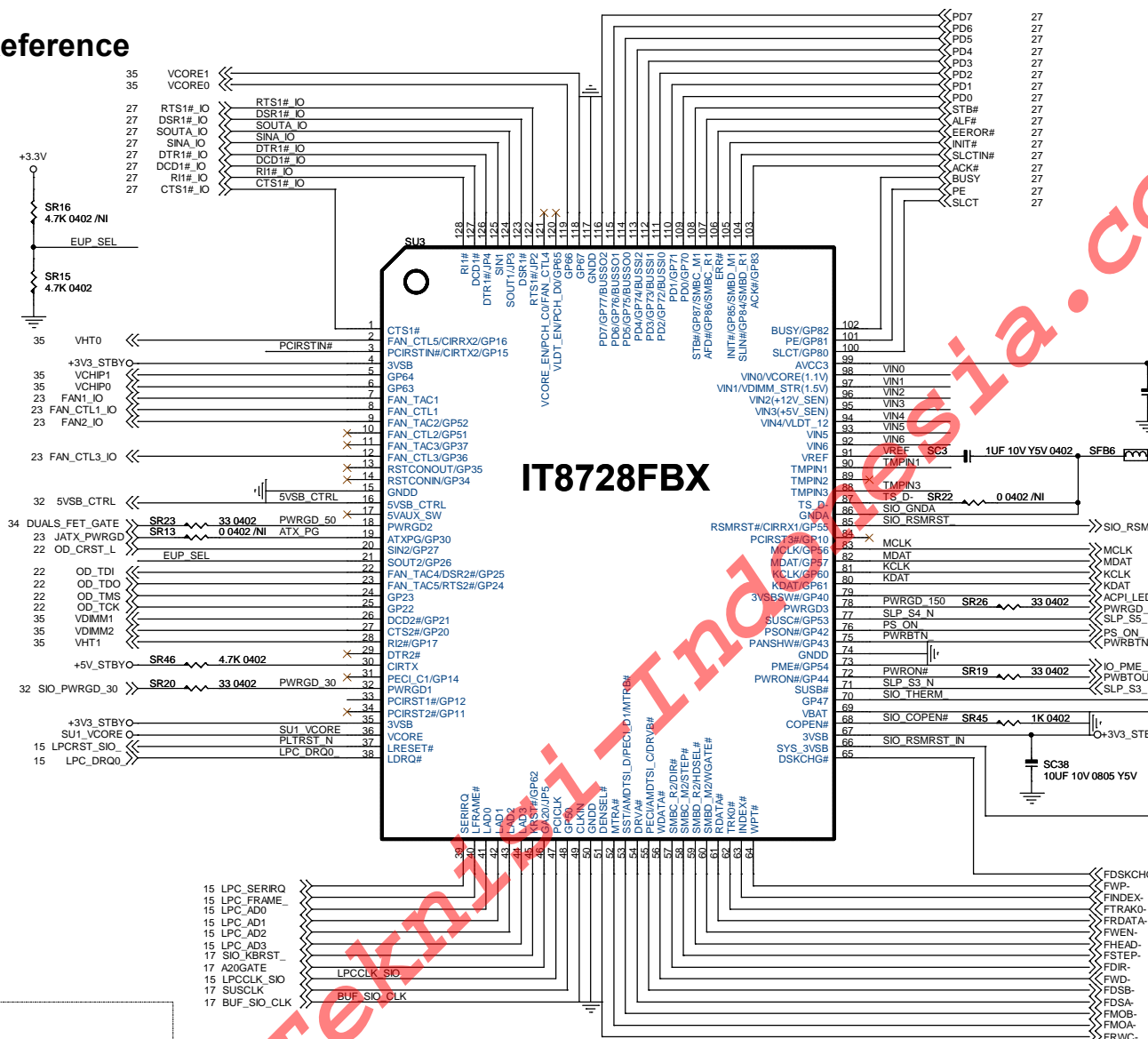
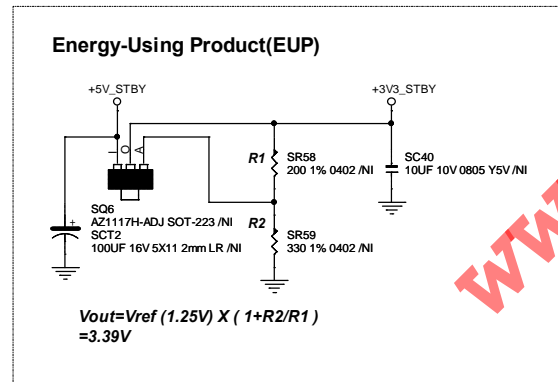
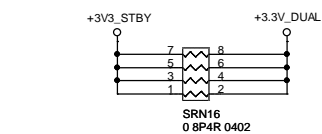
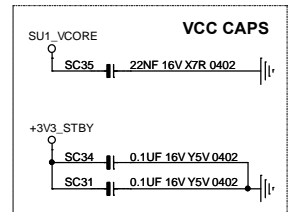
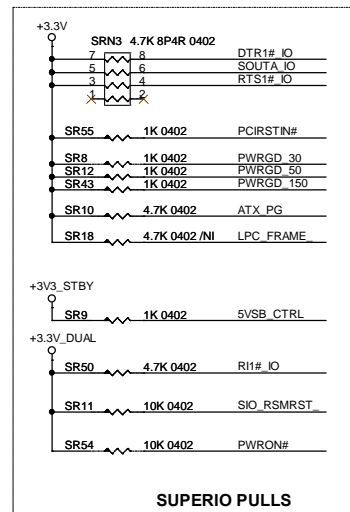
Rev 6.1







# SUPERIO PART: S+Reference



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File: LPC SUPER I/O IT8718

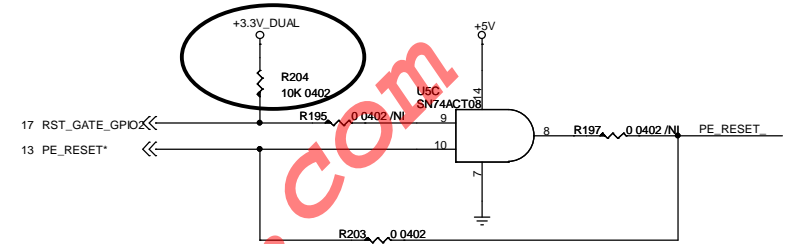
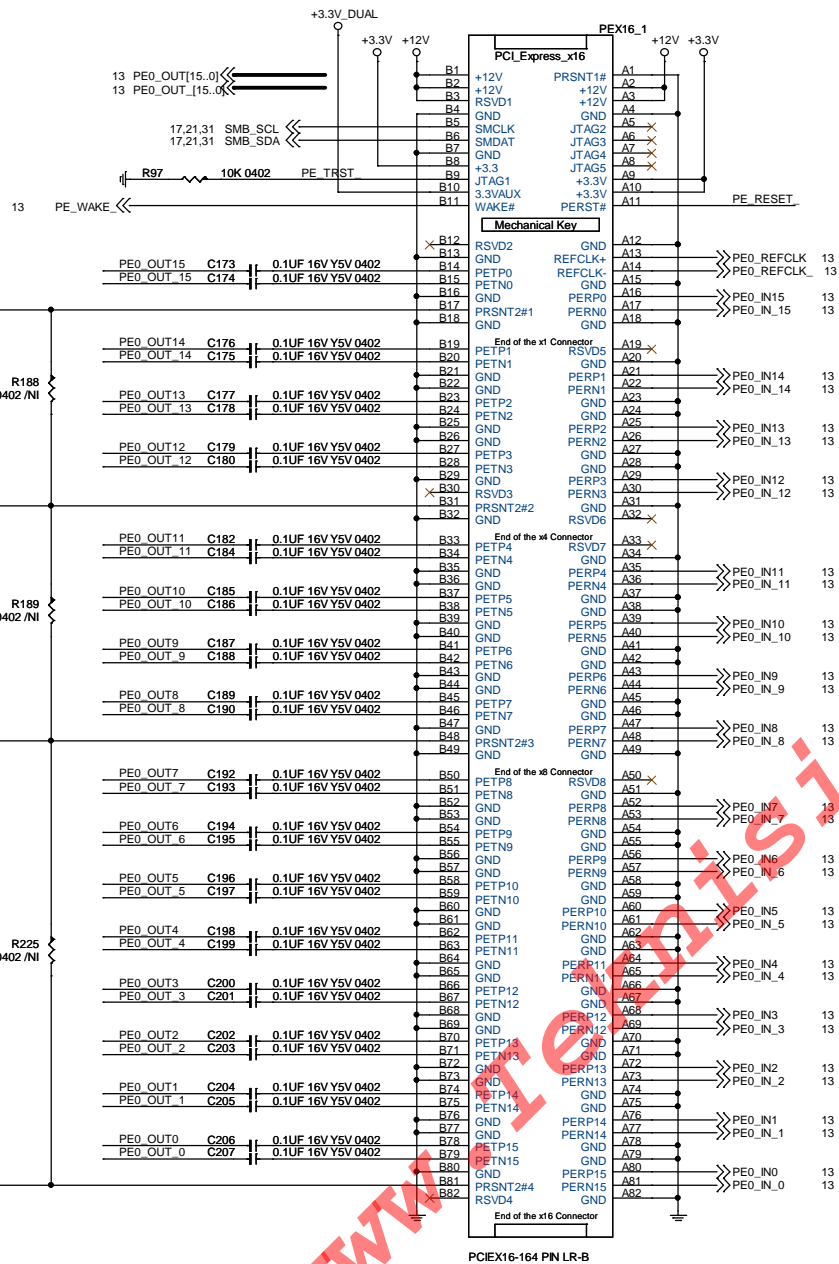
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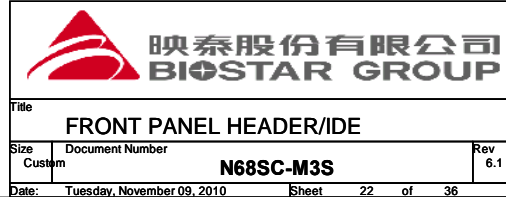
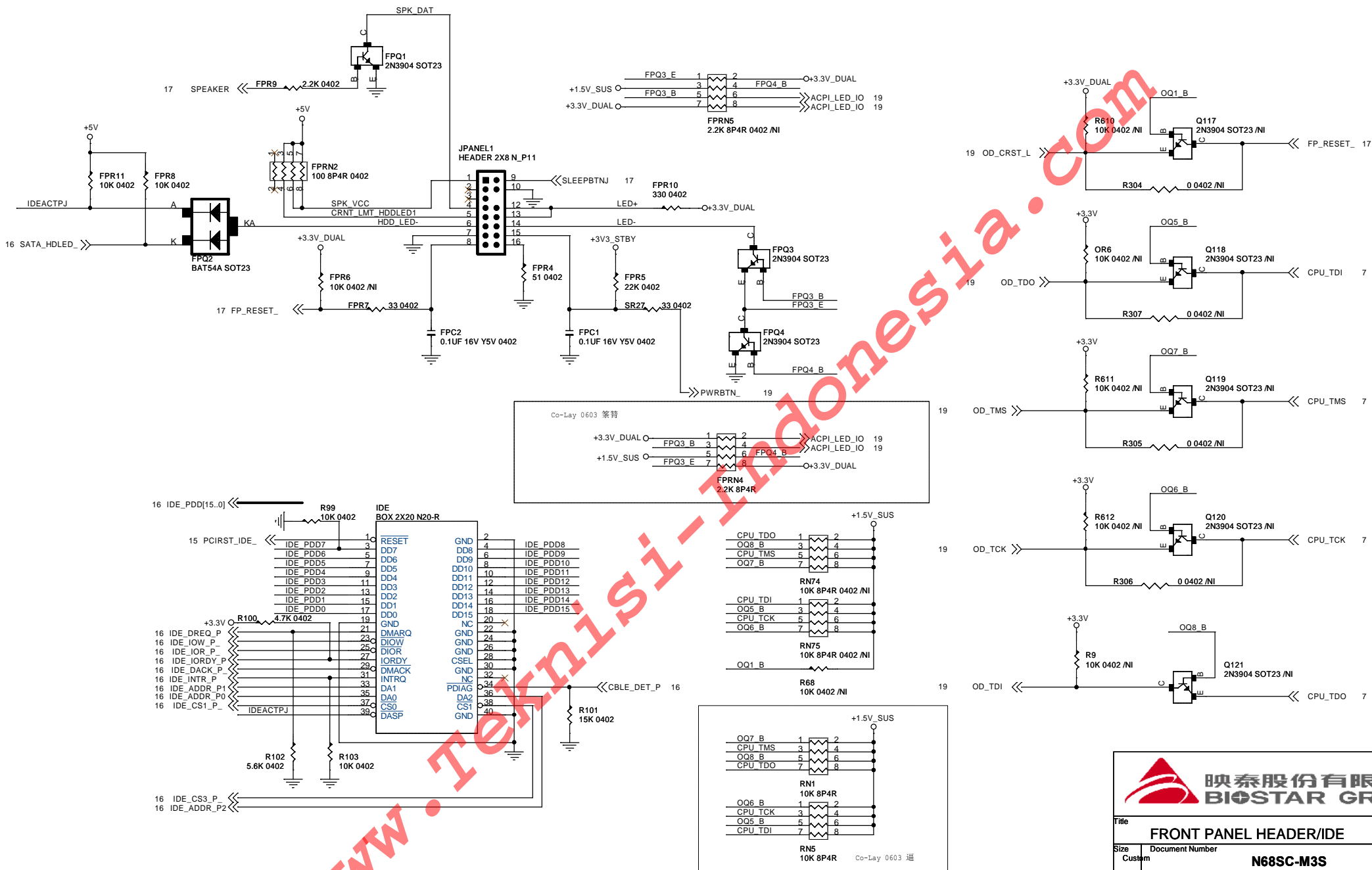
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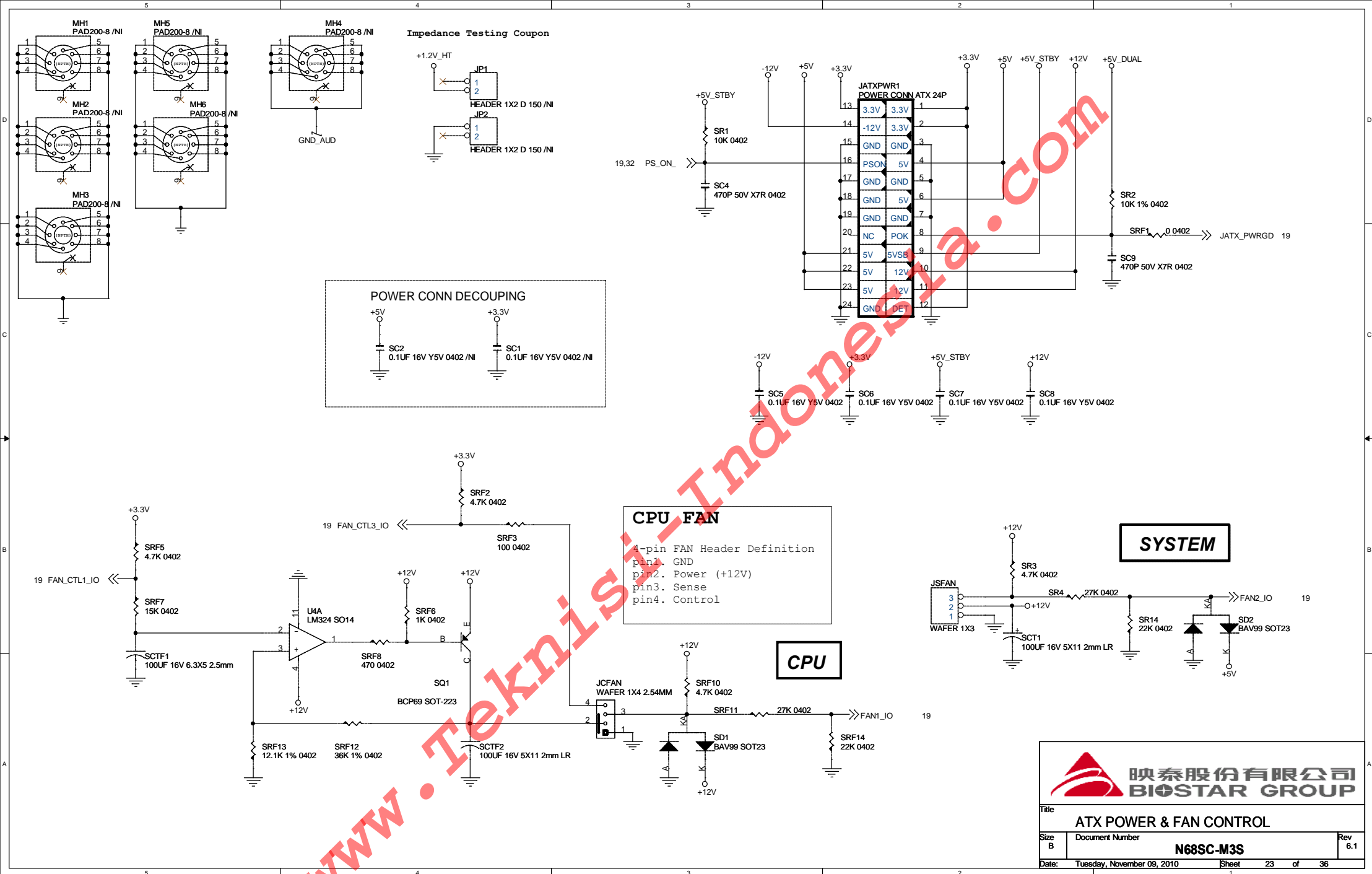
PCIEX16-164 PIN LR-B

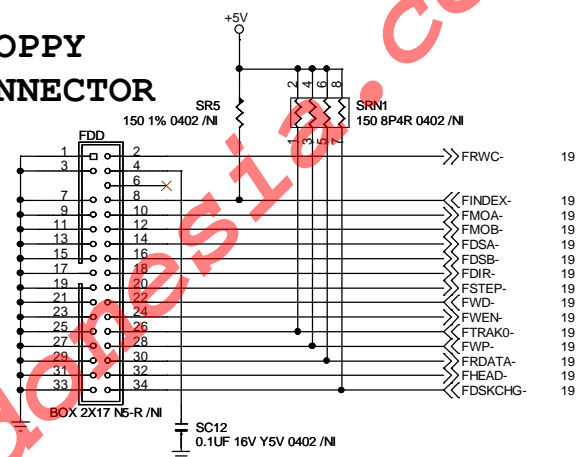
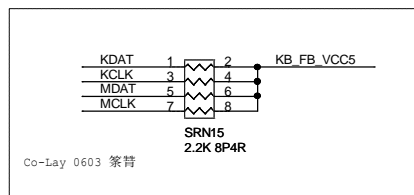
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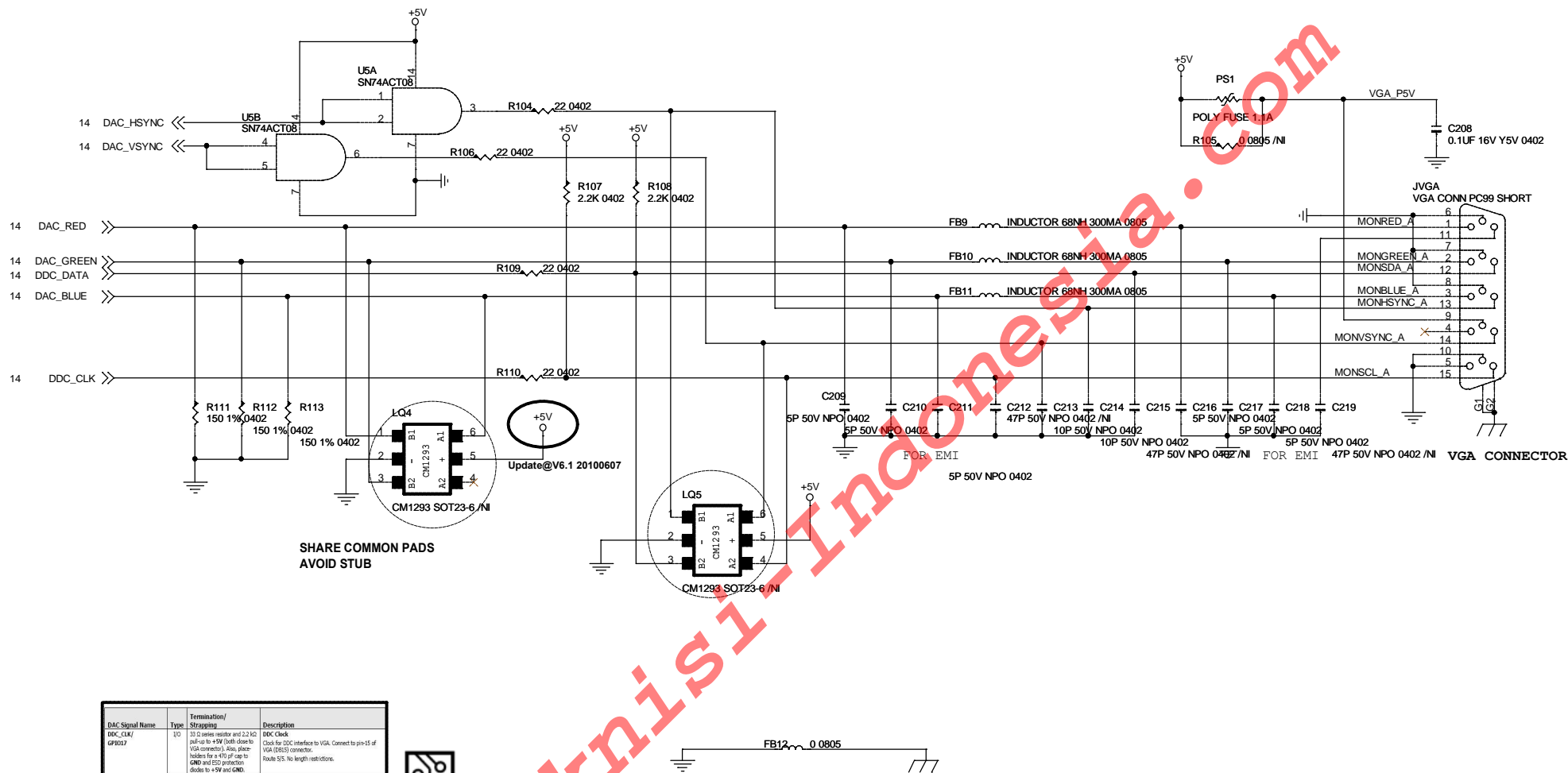




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DAC Signal Name	Type	Termination/Strapping	Description
DDC_CLK GP1017	I/O	33 Ω series resistor and 2.2 kΩ pull-up to +5V (both close to VGA connector). Also, place holder for a 470 pF cap to GND and ESD protection diodes to +5V and GND.	DDC Clock Clock for DDC interface to VGA. Connect to pin 15 of VGA (DB15) connector. Route 5/5. No length restrictions.
DDC_DATA/ GP1019	I/O	33 Ω series resistor and 2.2 kΩ pull-up to +5V (both close to VGA connector). Also, place holder for a 470 pF cap to GND and ESD protection diodes to +5V and GND.	DDC Data Data for DDC interface to VGA. Connect to pin 12 of VGA (DB15) connector. Route 5/5. No length restrictions.



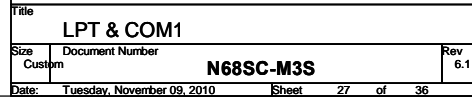
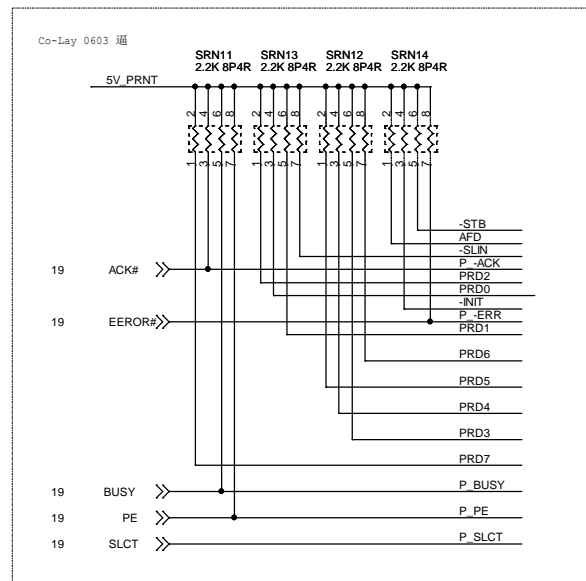
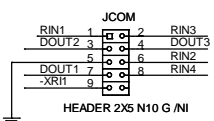

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Title <b>VGA CONNECTOR</b>		
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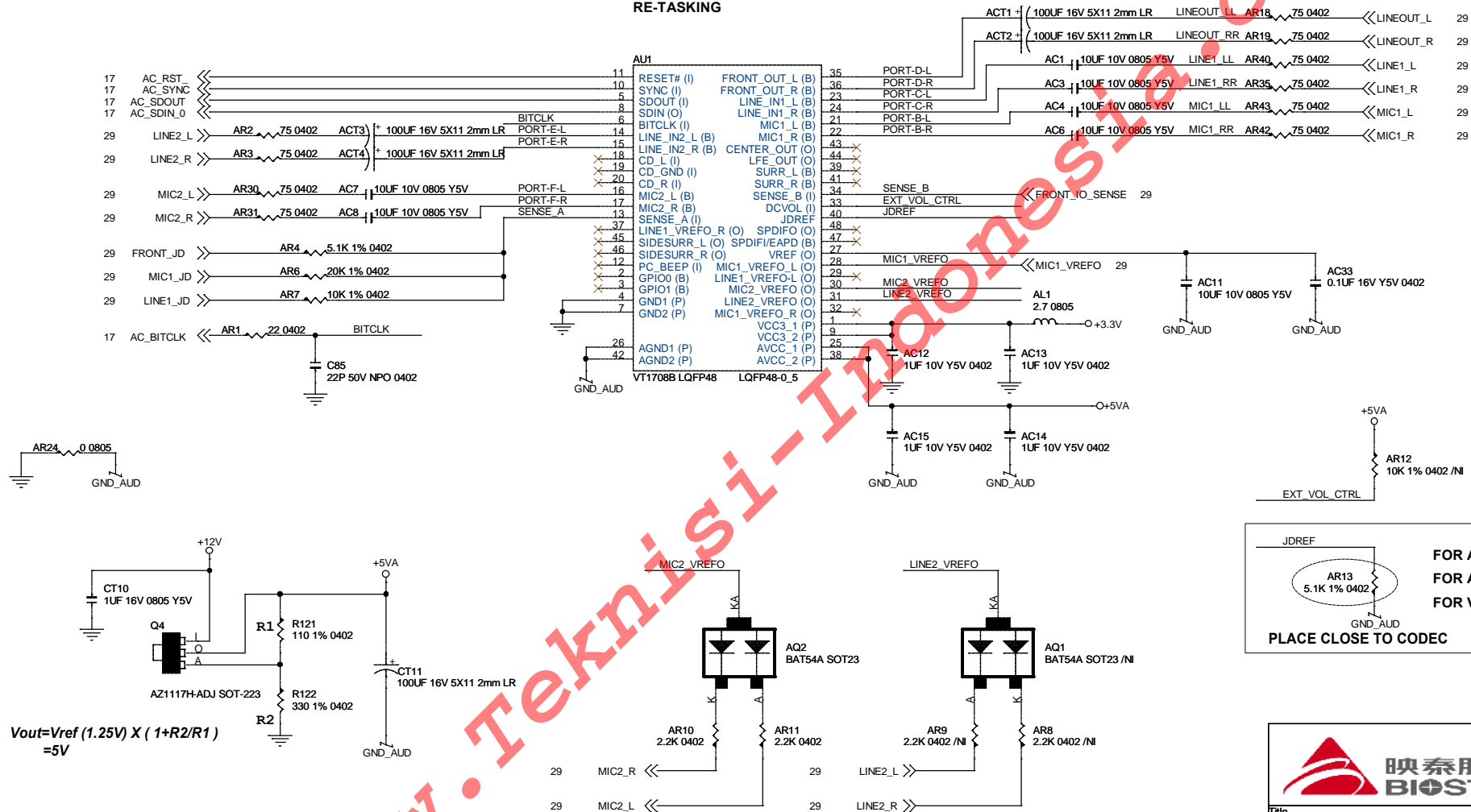


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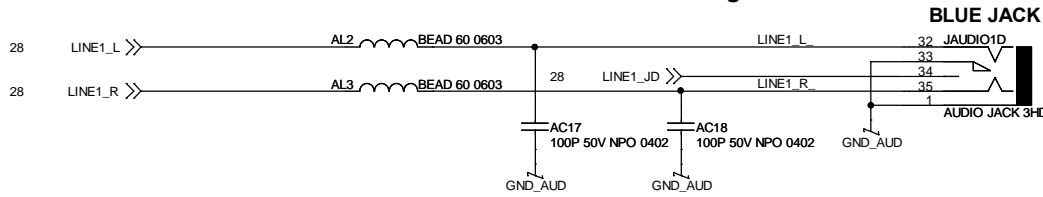


# CODEC ALC655/ALC658/ALC861VD/ALC883/VT1708A/ Colay Circuit

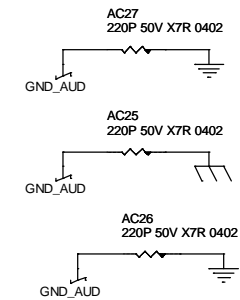
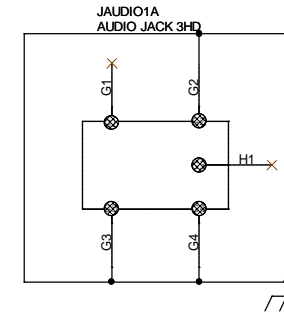
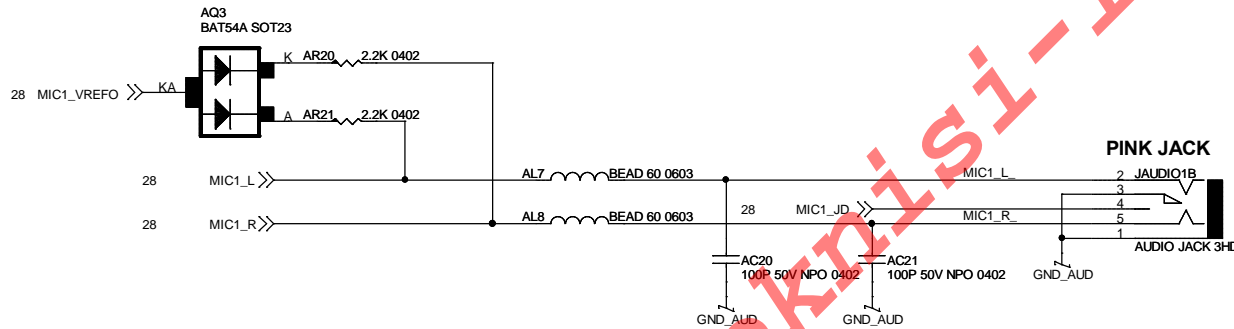
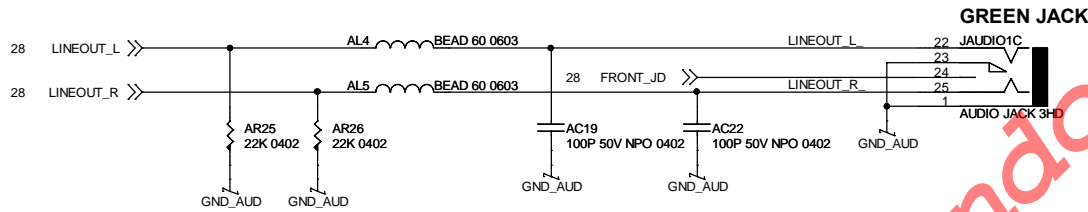
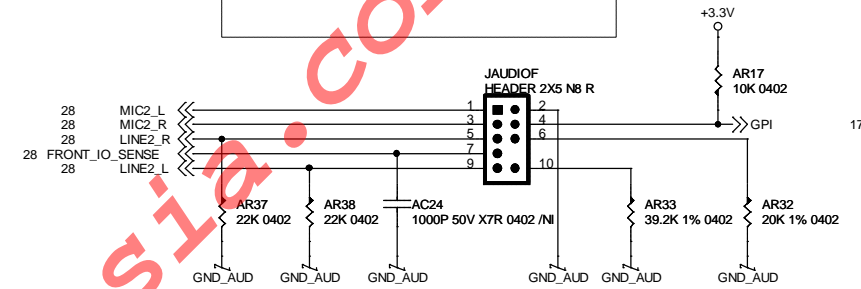
ALC861 : PORT D, E, F SUPPORT  
RE-TASKING(PIN#14, 15, 16, 17,  
35, 36)  
ALC888 : ALL PORTS SUPPORT  
RE-TASKING



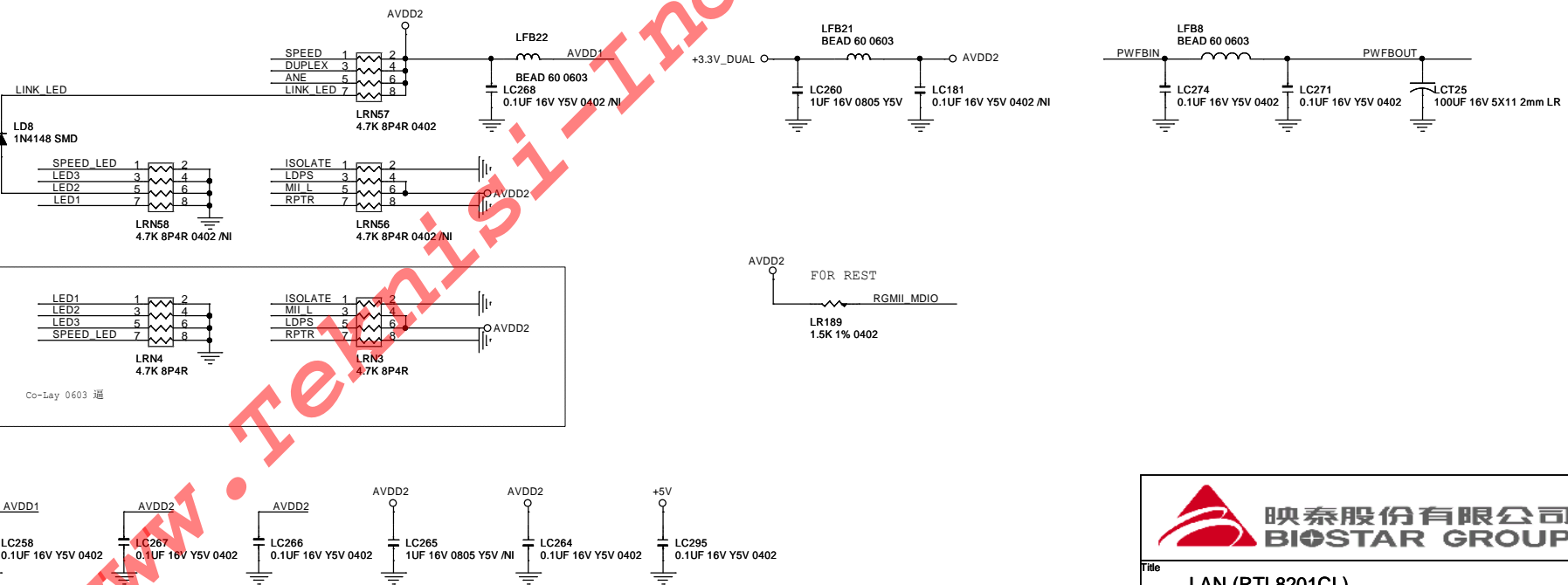
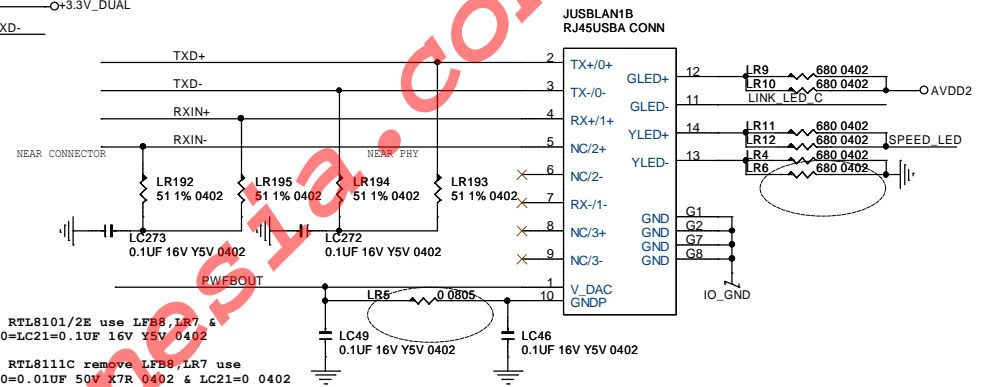
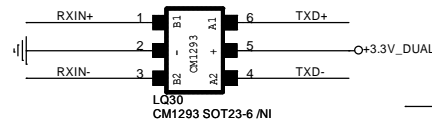
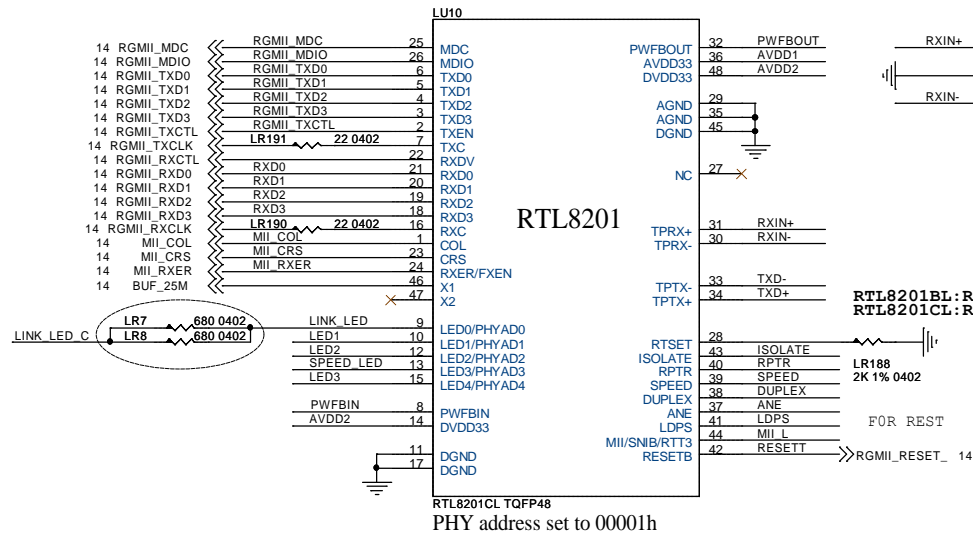
# Rear Panel Onboard Analog I/O



0: INTEL HD AUDIO DONGLE CONNECTED  
 1: INTEL HD AUDIO DONGLE UNCONNECTED



Title		
AUDIO PORT		
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R279 is reserved for 8201CL/CP LED Mode Change to compatible with BL

R280 is reserved for ensuring 8201BL/CL/CP latch to UTP Mode.

R281 is reserved for ensuring 8201CL/CP latch to normal operation mode.

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Title: LAN (RTL8201CL)

Size: Document Number

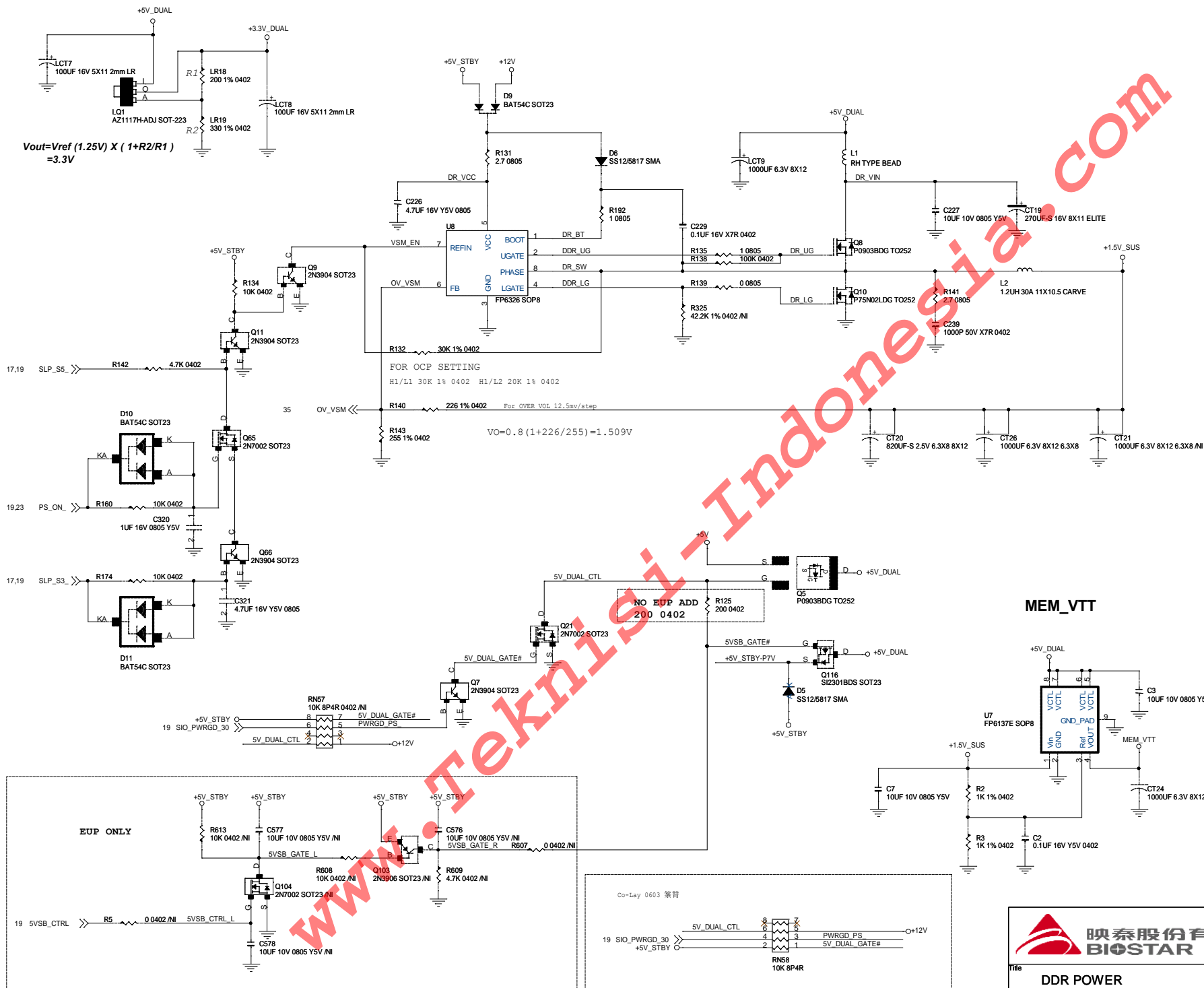
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Date: Tuesday, November 09, 2010

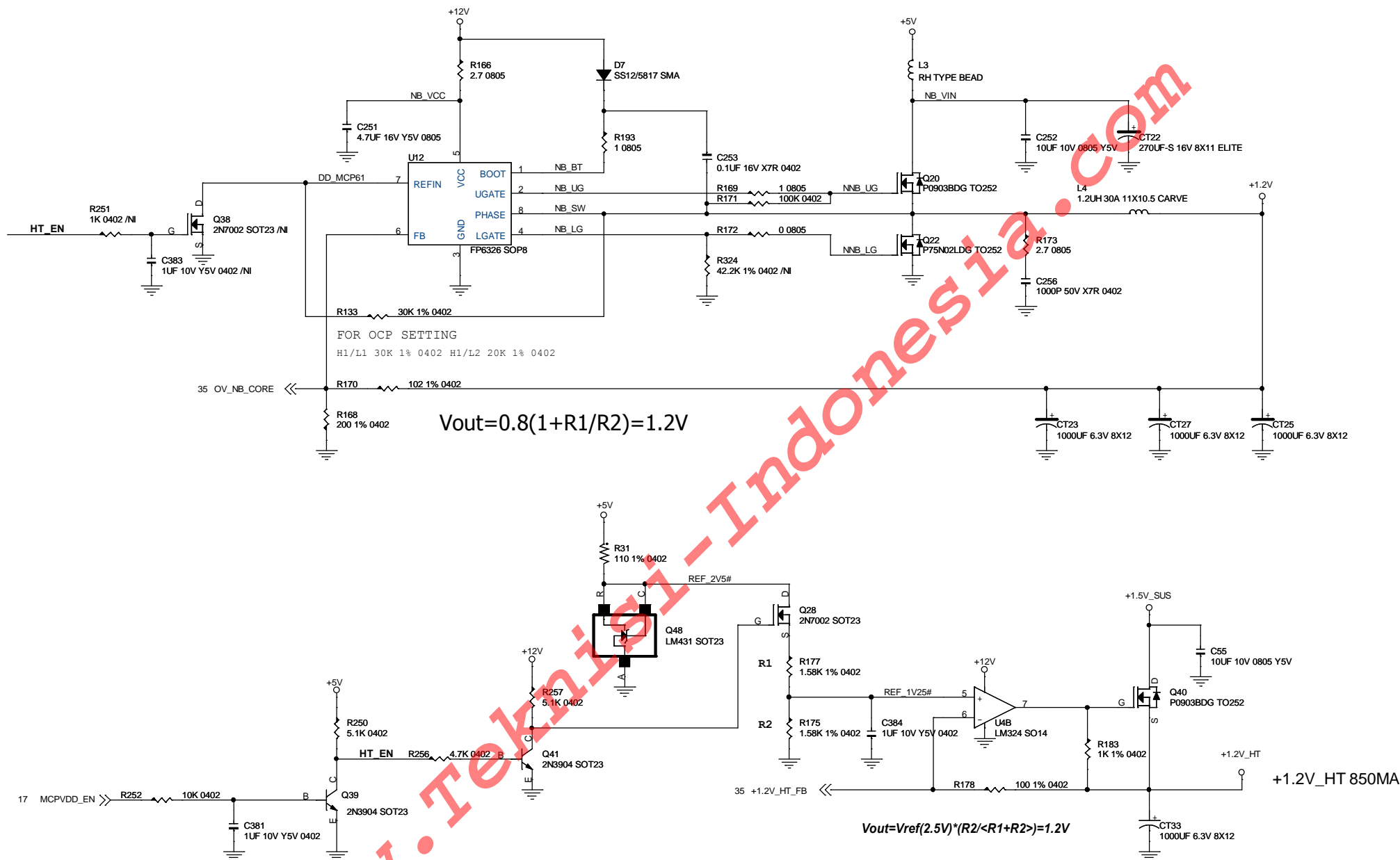
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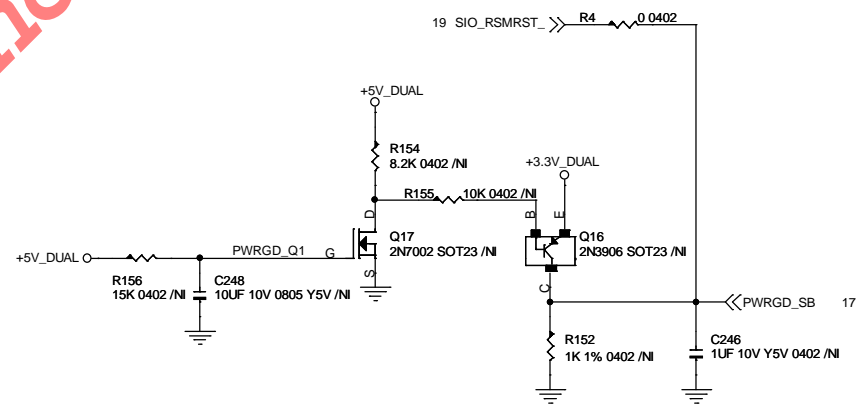
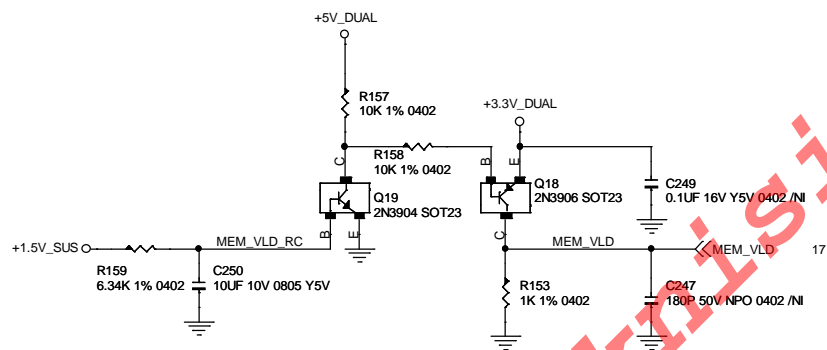
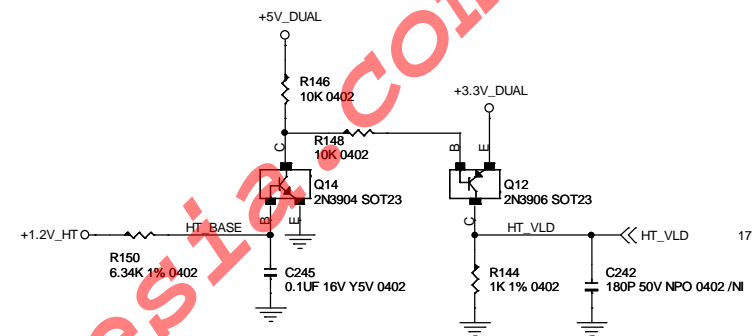
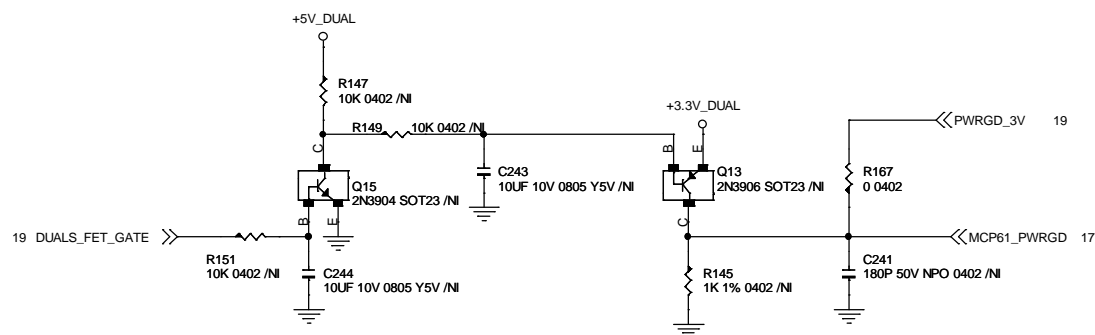




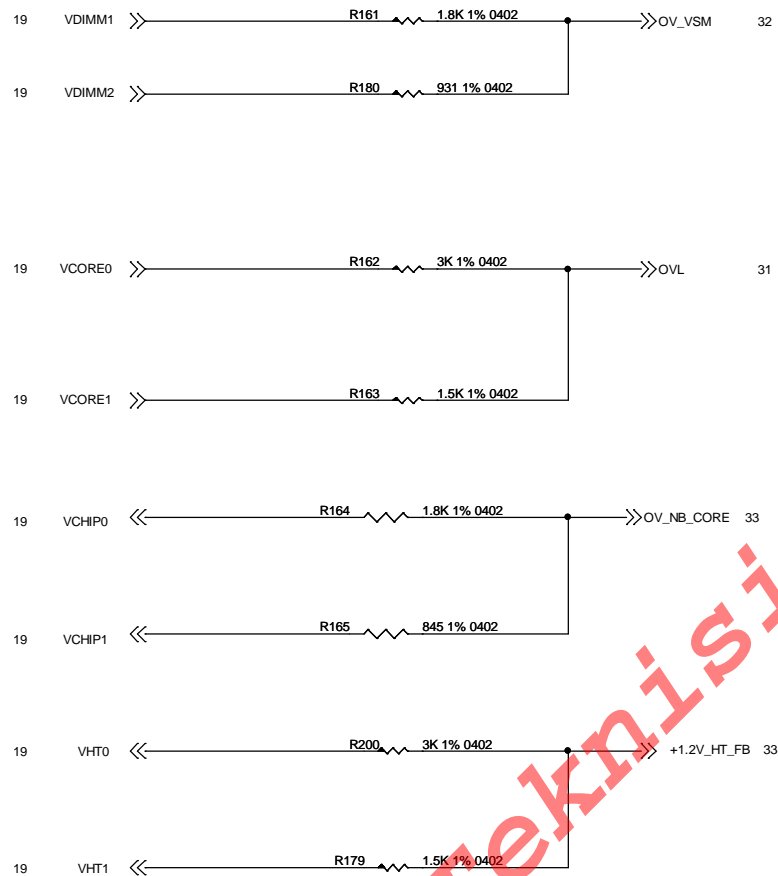




# POWER SEQUENCING



Title		
POWER SEQUENCING		
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VDIMM1	VDIMM2	VOLTAGE
HR	HR	+1.5V (Default)
0	HR	+1.6V
HR	0	+1.7V
0	0	+1.8V

VCORE_OVL	VCORE0	VCORE1
Default Vcore	HR	HR
Vcore(1%)	0	HR
Vcore(2%)	HR	0
Vcore(3%)	0	0

+1.2V	VCHIP0	VCHIP1
1.2V	HR	HR
1.25V	0	HR
1.3V	HR	0
1.35V	0	0

+1.2V_HT	VHT0	VHT1
1.25V	HR	HR
1.30V	0	HR
1.35V	HR	0
1.40V	0	0


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Title <b>OVER VOLTAGE</b>		
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JUSBPWR2(1\_2)  
JUMPER 2P R

JUSBPWR1(1\_2)  
JUMPER 2P R

JKB\_PWR(1\_2)  
JUMPER 2P R

(X2)  
XTAL WIRE



JCMOS1(1\_2)  
JUMPER 2P B

(BAT1)



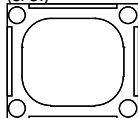
3V BATTERY SONY

(U2)



SPI MX25L8005 DIP

(CPU1)



AM2RM-B

(U1)



NBHS-A74GC

(PCB)



POLON 235X182

New JPANEL1  
JPANEL1 2\*11

PCB



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Title

BOM

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